ECEN 429: Introduction to Digital Systems Design Laboratory

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Pre Lab #10

**Introduction**

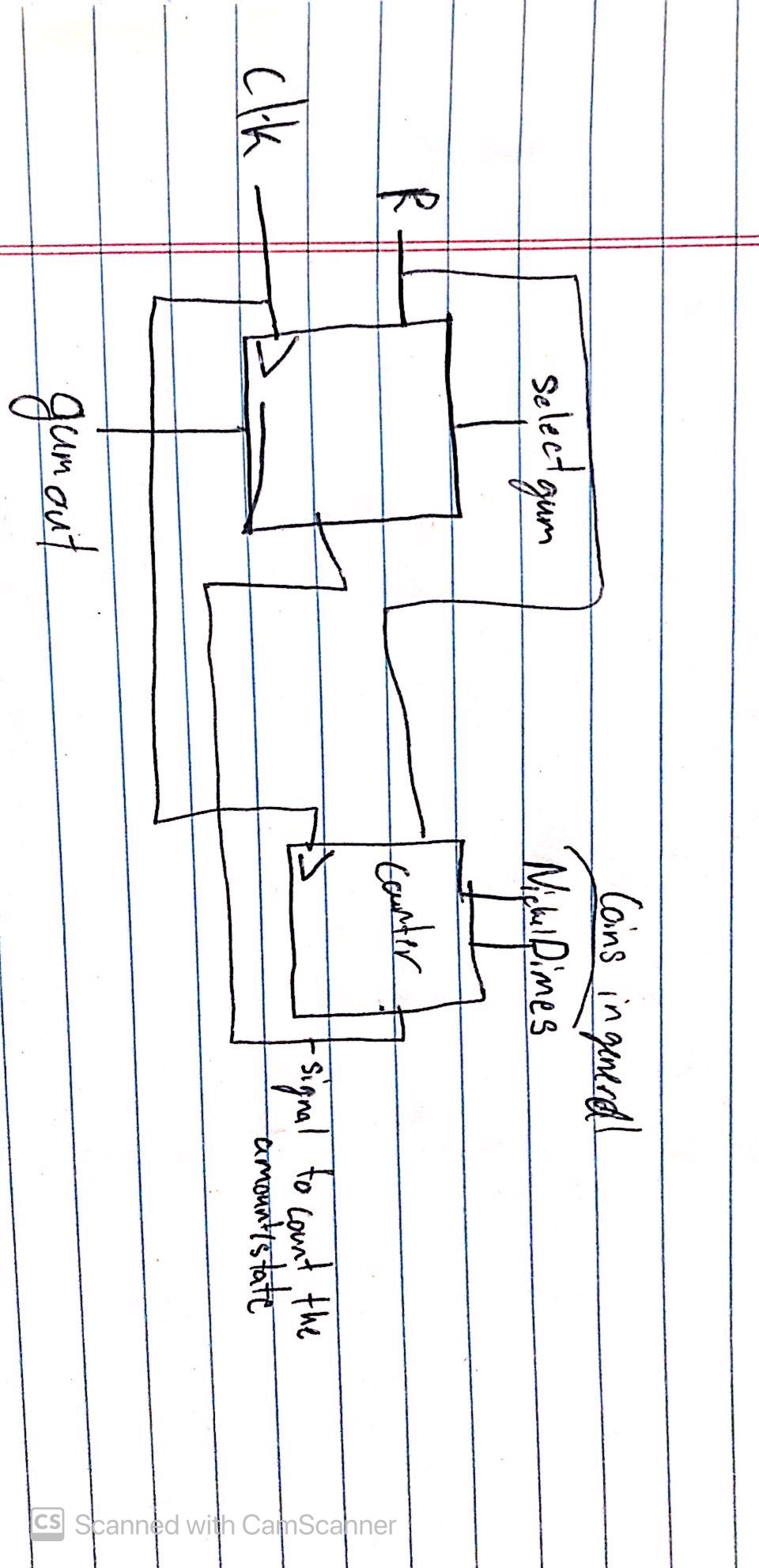
This prelab deals with doing vending machines.

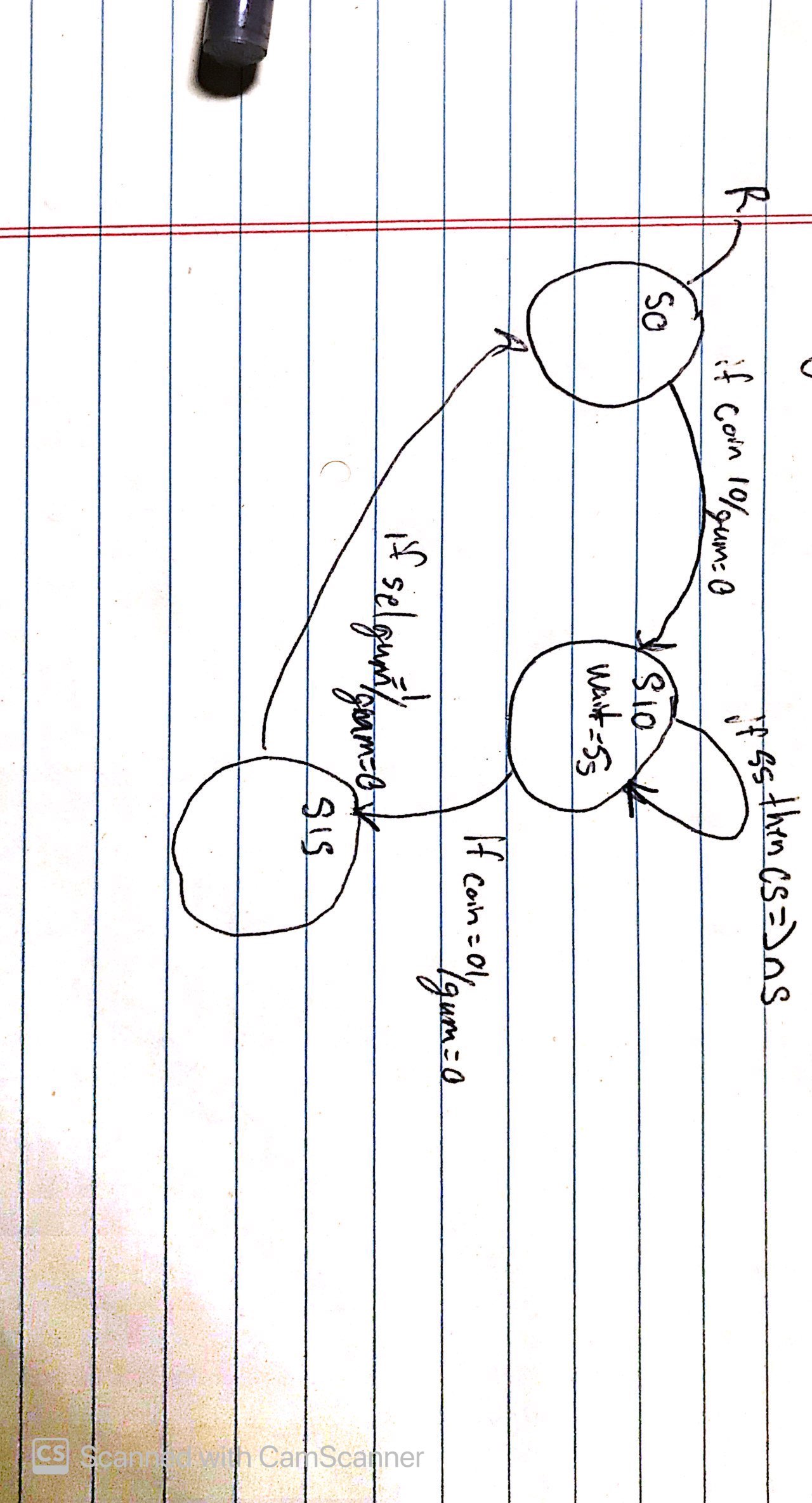
**Background, Design Solution and Results**

This prelab provides use insight into how a vending machine would work on the boards and what it entails in terms of the vhdl system.

Problem 1:

The inputs of the system would be based on two different components. A counter and vending machine fsm. The counter would include the input of the coin and an output that would tell the vending machine fsm how much money has been added so far. The vending machine fsm will have the input of the selection to buy the gum also a reset. The output of the vending machine would be the gum. The fsm should have to the logic within it to handle the timeout. Both components will be connected to a common clock.

Figure 1: top level desgin

Figure 2: state diagram

Entity vendingmachine is

Port(clk,r: in std\_logic;

Selgum: in std\_logic;

Coin: in std\_logic\_vector(1 downto 0);

Gumout: out std\_logic;

End;

Architecture beh of vendingmachine is

Type state is (S0,….S10,S15,timeout);

Signal cs,ns:state;

Signal Vtmp: std\_logic;

Signal timeouttmp: std\_logic;

begin

process(clk,r)

begin

if (r='1') then

cs<=s0;

elsif(clk'event and clk='1') then

cs<=ns;

end if;

end process;

process(coin,cs,selgum)

begin

case cs is

when S0=>

if (coin="00") then

ns<= cs;

elsif(coin="10") then

ns<=s10;

Vtmp= 0

Timeouttmp=0

When S10=>

If (coin=”01”) then

Ns<=S15;

if time>5s then

CS<=NS

When S15=>

If (sel=1) then

NS<=S0;

Vtmp=0

End ifs assumed;

Vtmp<=gumout;

Timeout<=timeouttmp;

End;

**Conclusion**

After doing the prelab, I understand the relationship between the vending machine and its components. The counter and the vendingmachine fsm have to work together to do fully operate the desired outcome.